CLAIMS

What is claimed is:

1. A circuit for use in a phase-locked loop (PLL) comprising:

a phase detector comprising:

first and second input circuits to generate first and second PLL control signals responsive to clock edges in first and second input signals, respectively; and

a reset circuit to generate a reset signal based on said first and second PLL control signals to reset said first and second input circuits; and

a cycle slip detector for each one of said first and second input circuits, each said cycle slip detector generating a slip indication signal based on said reset signal, a corresponding one of said first and second input signals, and a corresponding one of said first and second PLL control signals.

2. The circuit of claim 1 wherein each said cycle slip detector comprises slip detection logic to generate said slip indication signal when a clock edge in said corresponding one of said first and second input signals is received during said reset signal.

3. The circuit of claim 2 wherein said slip detection logic comprises a delay element to generate a delayed version of said reset signal, and wherein said slip detection logic additionally generates said slip indication signal in response to receiving a clock edge in said corresponding one of said first and second input signals when said delayed version of said reset signal is asserted.

4. The circuit of claim 1 wherein each said cycle slip detector comprises slip detection logic to generate said slip indication signal when a clock edge in said corresponding one of said first and second input signals is received when said corresponding one of said first and second PLL control signals is asserted.

5. The circuit of claim 2 wherein each said cycle slip detector comprises slip detection logic, said slip detection logic comprising:

an output flip-flop with a clock input coupled to said corresponding one of said first and second input signals; and

a logic gate with a first logic input coupled to said reset signal and a second logic input coupled to said corresponding one of said first and second PLL control signals, and with a logic output coupled to a data input of said output flip-flop, said logic gate operative to assert said logic output whenever at least one of said reset signal and said corresponding one of said first and second PLL control signals is asserted.

6. The circuit of claim 5 wherein said slip detection logic further comprises a delay element coupled to said reset signal and operative to generate a delayed version of said reset signal, said logic gate including a third logic input coupled to said delay element to receive said delayed version of said reset signal and operative to assert said logic output whenever said delayed version of said reset signal is asserted.

7. The circuit of claim 1 wherein each said first and second input circuits comprises a latching circuit generating a corresponding one of said first and second PLL control signals as a latched output signal responsive to a first clock edge in a corresponding one of said first and second input signals.

8. The circuit of claim 7 wherein said latching circuit comprises a reset input coupled to said reset signal and operative to reset said latched output signal when said reset signal is asserted so that said latching circuit responds to a next clock edge in said corresponding one of said first and second input signals.

9. The circuit of claim 7 wherein said latching circuit comprises an input flip-flop configured such that:

a data input of said input flip-flop is coupled to a fixed assertion signal;

a data output of said input flip-flop is coupled to an input of said reset circuit and to an input of said slip detection logic in a corresponding one of said cycle slip detectors;

a clock input of said input flip-flop is coupled to said corresponding one of said first and second input signals; and

a reset input coupled to a reset signal output of said reset circuit.

10. The circuit of claim 1 wherein said reset circuit comprises:

a logic gate with first and second inputs coupled to first and second PLL control signals from said first and second input circuits, and operative to assert an output signal when both said first and second control signals are asserted; and

a delay element to generate said reset signal a defined delay after assertion of said output signal from said logic gate.

11. A phase-locked loop (PLL) comprising:

a phase detector to generate first and second PLL control signals based on a detected phase difference between respective clock edges in first and second input signals, said phase detector comprising:

first and second input circuits to generate first and second PLL control signals responsive to clock edges in first and second input signals, respectively; and

a reset circuit to generate a reset signal based on said first and second PLL control signals to reset said first and second input circuits; and

a control circuit to generate a control signal based on said first and second PLL control signals;

a controllable oscillator to generate an output signal at a frequency based on said control signal; and

a first cycle slip detector to generate a first cycle slip indicator signal when a clock edge in said first input signal occurs during said reset signal; and

a second cycle slip detector to generate a second cycle slip indicator when a clock edge in said second input signal occurs during said reset signal;

wherein said first input signal is derived from a reference clock signal and said second input signal is derived from a frequency-controlled output of said PLL.

12. The PLL of claim 11 wherein said first and second cycle slip detectors each comprise slip detection logic, said slip detection logic comprising:

an output flip-flop with a clock input coupled to a corresponding one of said first and second input signals; and

a logic gate with a first logic input coupled to said reset signal and a second logic input coupled to a corresponding one of said first and second PLL control signals, and with a logic output coupled to a data input of said output flip-flop, said logic gate operative to assert said logic output whenever at least one of said reset signal and said corresponding one of said first and second PLL control signals is asserted.

13. The PLL of claim 12 wherein said slip detection logic further comprises a delay element coupled to said reset signal and operative to generate a delayed version of said reset signal, said logic gate including a third logic input coupled to said delay element to receive said delayed version of said reset signal and operative to assert said logic output whenever said delayed version of said reset signal is asserted.

14. The PLL of claim 11 wherein each said first and second input circuits comprises a latching circuit generating a corresponding one of said first and second PLL control signals as a latched output signal responsive to a first clock edge in a corresponding one of said first and second input signals.

15. The PLL of claim 14 wherein said latching circuit comprises a reset input coupled to said reset signal and operative to reset said latched output signal when said reset signal is asserted so that said latching circuit responds to a next clock edge in said corresponding one of said first and second input signals.

16. The PLL of claim 14 wherein said latching circuit comprises an input flip-flop configured such that:

a data input of said input flip-flop is coupled to a fixed assertion signal;

a data output of said input flip-flop is coupled to an input of said reset circuit and to an input of said slip detection logic in a corresponding one of said cycle slip detectors;

a clock input of said input flip-flop is coupled to said corresponding one of said first and second input signals; and

a reset input coupled to a reset signal output of said reset circuit.

17. A radio transceiver comprising:

a receiver to receive a remotely transmitted signal at a receive frequency;

a transmitter to generate a transmit signal at a carrier frequency; and

a frequency synthesizer to generate a first output signal bearing on said receive frequency and a second output signal bearing on said carrier frequency, said frequency synthesizer comprising:

a reference clock circuit to generate a reference clock signal; and

first and second phase-locked loops (PLLs) to generate said first and second output signals, respectively, at least one of said first and second PLLs comprising:

a phase detector to generate first and second PLL control signals based on a detected phase difference between respective clock edges in first and second input signals, said first input signal derived from said reference clock signal and said second input signal derived from a corresponding one of said first and second output signals from said frequency synthesizer, said phase detector comprising:

first and second input circuits to generate first and second PLL control signals responsive to clock edges in first and second input signals, respectively; and

a reset circuit to generate a reset signal based on said first and second PLL control signals to reset said first and second input circuits; and

a control circuit to generate a control signal based on said first and second PLL control signals;

a controllable oscillator to generate said corresponding one of said first and second output signals at a frequency based on said control signal; and

a first cycle slip detector to generate a first cycle slip indicator signal when a clock edge in said first input signal occurs during said reset signal; and

a second cycle slip detector to generate a second cycle slip indicator when a clock edge in said second input signal occurs during said reset signal.

18. The radio transceiver of claim 17 wherein said first and second cycle slip detectors each comprise slip detection logic, said slip detection logic generating a corresponding one of said first and second cycle slip indicator signals when a clock edge is received in a corresponding one of said first and second input signals while at least one of said reset signal and a corresponding one of said first and second PLL control signals is asserted.

19. A method of detecting cycle slip in a phase detector circuit, the method comprising:

operating said phase detector to generate first and second PLL control signals based on latching respective first clock edges in first and second input signals;

resetting said phase detector with a reset pulse after both said first clock edges occur to make said phase detector responsive to next clock edges in said first and second input signals;

generating a slip indicator signal in response to said next clock edge occurring in at least one of said first and second input signals before said reset pulse, and in response to any clock edge in at least one of said first and second input signals occurring during said reset pulse.

20. The method of claim 19 wherein generating a slip indicator signal in response to said next clock edge occurring in at least one of said first and second input signals before said reset pulse, and in response to any clock edge in at least one of said first and second input signals occurring during said reset pulse comprises:

generating a first cycle slip indicator signal if said next clock edge occurs in said first input signal before said reset pulse, and if said any clock edge occurs in said first input signal during said reset pulse; and

generating a second cycle slip indicator signal if said next clock edge occurs in said second input signal before said reset pulse, and if said any clock edge occurs in said second input signal during said reset pulse.

21. The method of claim 19 further comprising:

deriving a delayed reset pulse from said reset pulse;

detecting whether any clock edges occur in at least one of said first and second input signals during said delayed reset pulse; and

generating said cycle slip indicator signal in response to said any clock edges occurring during said delayed reset pulse.

22. The method of claim 19 further comprising determining whether a missed clock edge is an up-cycle slip or a down-cycle slip based on determining whether said phase detector misses a clock edge in said first input signal or in said second input signal, respectively.

23. The method of claim 22 further comprising generating said cycle slip indicator signal as an up-cycle slip indicator upon occurrence of said up-cycle slip and generating said cycle slip indicator signal as a down-cycle slip indicator upon occurrence of said down-cycle slip.

24. The method of claim 22 further comprising:

deriving a delayed reset pulse from said reset pulse;

detecting whether a clock edge occurs in said first input signal during said delayed reset pulse;

generating said up-cycle slip indicator in response to said clock edge occurring in said first input signal during said delayed reset pulse;

detecting whether a clock edge occurs in said second input signal during said delayed reset pulse; and

generating said down-cycle slip indicator in response to said clock edge occurring in said second input signal during said delayed reset pulse.